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RAPID COMMUNICATION

Monolithically integrated thermoelectric energy harvester based on silicon nanowire arrays for powering micro/nanodevices

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Abstract
One-dimensional (1D) nanowire structures have been shown to be promising candidates for enhancing the thermoelectric properties of semiconductor materials. This paper goes beyond single nanowire characterization and reports on the implementation of multiple electrically connected dense arrays of well-oriented and size-controlled silicon nanowires (Si NWs) grown by the CVD-VLS mechanism into microfabricated structures to develop thermoelectric microgenerators (μTEGs). Low thermal mass suspended silicon structures have been designed and microfabricated to naturally generate thermal gradients in planar microthermoelements. The hot and cold parts of the device are linked with horizontal arrays of Si NWs growth by a single bottom-up process. In order to improve the performance of the device as energy harvester, the successive linkage of multiple Si NW arrays has been developed to generate larger temperature differences while preserving a good electrical contact that allows keeping small internal thermoelement resistances. The fabricated thermoelements have shown Seebeck voltages up to 60 mV and generated power densities up to 1.44 mW/cm^2 for $\Delta T = 300\ ^\circ C$ and, working as energy harvesters, a maximum Seebeck voltage of 4.4 mV and a generated power density of 9 μW/cm^2 for $\Delta T = 27\ ^\circ C$ (across the nanowires) in a single thermoelement. The fabricated microgenerator, taking advantage of the simple planar geometry and compatibility with silicon technology, provides an alternative to the state-of-the-art μTEGs based on non-integrable and scarce V–VI semiconductor materials and a promising energy harvester for advanced micro/nanosystems.

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Introduction

The increasing world's demand for ubiquitous power generation is driving the development of new materials and technologies able to extract energy from the environment. For ambient energy sources such as vibrational, solar or thermal, the power density that can be harvested is in the range of tenths of microwatts to miliwatts per cubic centimeter [1], i.e. high enough for powering small electronics, nodes in wireless sensor networks or remote actuators. However, these applications usually involve scaling down the generators to the microscale by using MEMS technology, therefore limiting the materials allowed for their fabrication. Furthermore, recently discovered nanodevices fabricated with one-dimensional nanostructures [2,3], regardless of having low-power requirements, call for power sources compatible to nano- or micro-electronic technologies in order to take advantage of their size [4,5].

Thermoelectric generators (TEGs) are devices able to harvest waste heat directly converting it into electricity. Due to their adaptability to different thermal gradients and energy densities as well as good scalability from μW to hundreds of kW, thermoelectric generators are particularly interesting for powering portable devices [6]. However, the poor thermoelectric properties of materials traditionally used in microelectronics (*e.g.* silicon with $ZT \sim 0.01$) and the poor compatibility of good thermoelectric materials (*e.g.* Bi_2Te_3) with mainstream microelectronics have limited their integration [7]. In addition to the non-CMOS compatibility of the commercially available state-of-the-art thermoelectric materials, they are usually scarce and expensive compounds based on Bi, Te, Sb, Se and Pb that suffer from short-term high supply risk [8].

Recent results showing a great enhancement of the thermoelectric properties in low-dimensional semiconductors by quantum confinement and phonon scattering effects offer a promising approach to open the range of semiconductor materials for thermoelectric power generation [9,10]. In particular, Boukai et al. [11] and Hochbaum et al. [12] proved that one-dimensional silicon nanostructures present greatly enhanced thermoelectric properties compared to bulk silicon. An improvement of the figure of merit (ZT) of nanostructured silicon was achieved due to an important reduction of the thermal conductivity without much affecting the Seebeck coefficient and the electrical resistivity [11–16]. These significant studies open up the opportunity to use silicon, in the form of silicon nanowires (Si NWs), for thermoelectric applications. Nevertheless, although silicon represents a great advantage from a technological point of view, large-scale integration of Si NW-based devices still remains a challenge due to the compatibility difficulties between the 2D dominant planar architecture of microdevices and the 3D nature of nanowire growth, and to the critical issue of assuring the electrical accessibility of the nanowires without resourcing to complex handling and post-processing steps. In this work, the electrical accessibility and spatial constraints issues have been solved by combining an appropriate device geometry, defined by top-down silicon micromachining, with a controlled bottom-up lateral growth of well oriented Si NWs using the chemical vapor deposition (CVD) technique [17–19]. Low thermal mass suspended structures have been designed and microfabricated to naturally generate thermal gradients and operate as microgenerators using monolithically integrated *p*-type bottom-up silicon nanowire arrays as the active thermoelectric material. In order to obtain high thermal gradients a metamaterial based on multiple ordered arrays consecutively linked by means of transversal microspacers has been defined and implemented. The multiple-array planar approach presented here could represent a step forward towards silicon-based thermoelectric generation for energy harvesting applications in advanced micro/nanodevices.

Device design

The operation principle of the proposed thermoelectric microgenerator (μTEG) is depicted in Figure 1a. The μTEG is based on an architecture consisting of a thermocouple with a leg of a *p*-type Si NW array (acting as nanostructured thermoelectric material) and another one of tungsten. This architecture is usually referred to as "uni-leg" since only a single polarity semiconductor is used as thermoelement. In this planar design, a suspended silicon platform (S1) is connected to the silicon bulk (S2) through low thermal mass silicon bridges, allowing the natural generation of a temperature difference between the platform and the bulk

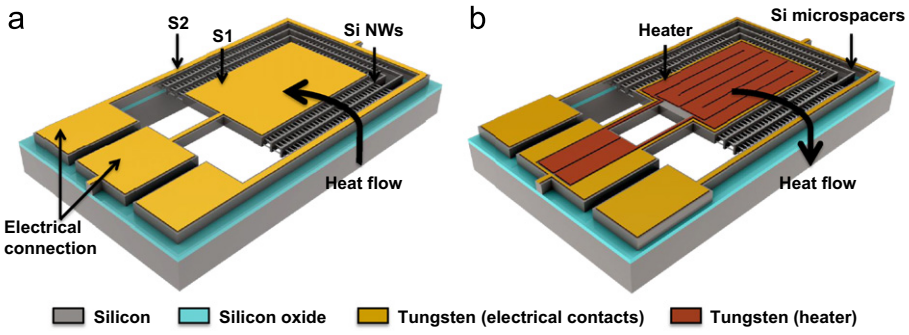

Figure 1 Sketch showing the design of the basic structure. (a) A thermally isolated suspended silicon mass (S1) is connected to the surrounding silicon bulk (S2) through silicon nanowires (Si NWs) allowing a planar temperature difference to be achieved, conforming in this way a thermoelement in which the Si NWs act as a nanostructured thermoelectric material; (b) sketch of a similar device showing an integrated heater employed both as heat source and sensor to control and characterize the temperature gradients attainable in the structure. Heat flow is reversed in this configuration.

when this one is in contact with a heat source. In addition to the supporting silicon beams, these high and low temperature areas are physically connected by the Si NW arrays. The temperature difference attainable across the thermoelectric legs depends on the actual length of the connecting nanowires, which can be technologically limited due to tapering effects during their growth [20-23]. Microstructures composed by multiple ordered arrays consecutively bridged by transversal microspacers have been implemented to overcome this problem, leading to larger effective Si NW lengths. This approach simplifies growth optimization and helps to build a flexible and mechanically robust device. The proposed geometry has been tested with an intermediate proof-of-concept structure including a heater in the suspended platform (Figure 1b). Although the presence of the heater imposes an area penalty to the device and worsens the thermal isolation of S1, it allows an easier and more flexible device thermal characterization enabling the analysis of the thermoelement under large thermal gradients [24].

Results and discussion

Figure 2 schematically illustrates the fabrication process of the μTEG structures (experiment details are provided in Appendix A). Square suspended platforms (500×500 μm) have been defined starting from a silicon-on-insulator (SOI) wafer with a 15 μm (110) *p*-doped silicon device layer. PECVD oxide passivated silicon platforms and microspacers were defined by two deep reactive ion etching steps (DRIE, from the top and the bottom of the wafer) using the SOI buried oxide as an etch stop. A tungsten layer was employed to pattern the characterization heater and the pads and connections giving electrical access to the structures. This metallization process proved pivotal for the Vapor-Liquid-Solid (VLS) Si NW-based device integration [25]. The device was designed in such a way that only (111) planes, where the nanowires would preferentially grow, were exposed by the DRIE of the silicon device layer. The selective growth of nanowires in these sidewalls was achieved by means of the galvanic displacement method, which was used to control the deposition of the Au catalyst nanoparticles, seed of the CVD-VLS process, only at silicon exposed surfaces [26,27]. The transversal microspacers designed to consecutively bridge several horizontal 10 μm-long nanowire arrays consisted of 3 μm-width silicon beams.

Figure 3a shows a SEM image of the whole fabricated μTEG sketched in Figure 1b. Multiple linked nanowire arrays were achieved by horizontally synthesizing in situ *p*-doped silicon nanowires between these opposing (111) sidewalls (Figure 3b and c) obtaining nanowires with an average diameter of 100 nm. A high-resolution TEM analysis was performed to verify the crystalline growth of silicon nanowires (Figure 3d). Four designs based on a different number of microspacers bridging 1, 3, 6 and 9 arrays of silicon nanowires were placed in the same chip allowing to obtain different nanowire effective lengths in a single bottom-up growth process. The arrangement of a different number of arrays consecutively linked can be understood as metamaterial, constructed rather than synthesized, with given thermal and electrical properties. This metamaterial can

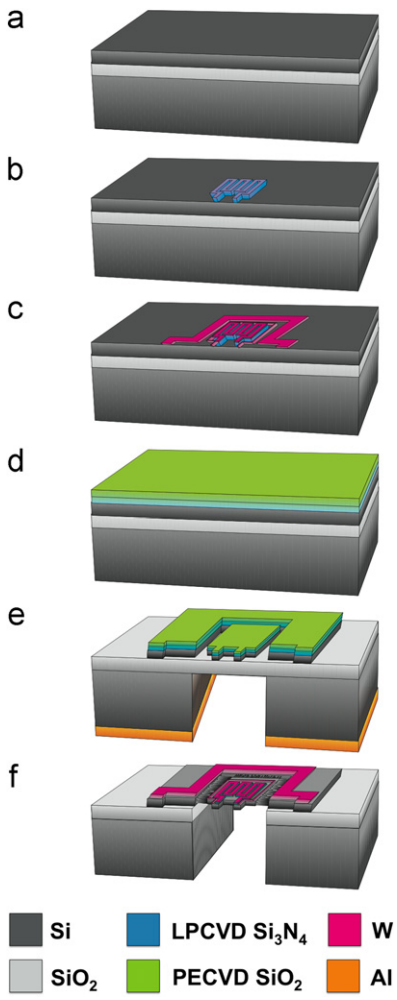

Figure 2 Main steps of the microfabrication process flow of planar thermoelectric generators. (a) SOI wafers with a 15 μm-thick Si (110) device layer and a 1 μm-thick buried thermal SiO_2 layer were employed; (b) the fabrication process started with a Low-Pressure CVD (LPCVD) nitride layer patterned to electrically isolate the heater from the suspended platform (S1); (c) a 1500 Å-thick tungsten layer and a lift-off process were used to define the heater and electrical contacts; (d) a 5000 Å-thick Plasma-Enhanced CVD (PECVD) SiO_2 layer was used to ensure Si NWs growth only at exposed silicon areas, passivating certain silicon and metal areas during the growth process; (e) the silicon device layer and the SiO_2 passivation layer were simultaneously etched to define the main geometry of the device, the microspacers and the (111) silicon sidewalls for nanowire growth. A Deep Reactive Ion Etching (DRIE) process was performed to etch the backside of the wafer in order to suspend the platform of the device (S1) using an aluminum layer as mask; (f) wafers were cut and silicon nanowire growth was performed at a chip-level. As a final step, the buried oxide layer of the SOI wafer and the passivation layer were etched.

be regarded as a bottom-up ultra high-density version of the top-down nanomesh concept developed by Yu et al. [28].

To electrically measure the device temperature, the heaters patterned on it were employed as thermometers. For this purpose, the temperature coefficient of resistance (TCR) of tungsten was measured to be 1920 ± 20 ppm/°C

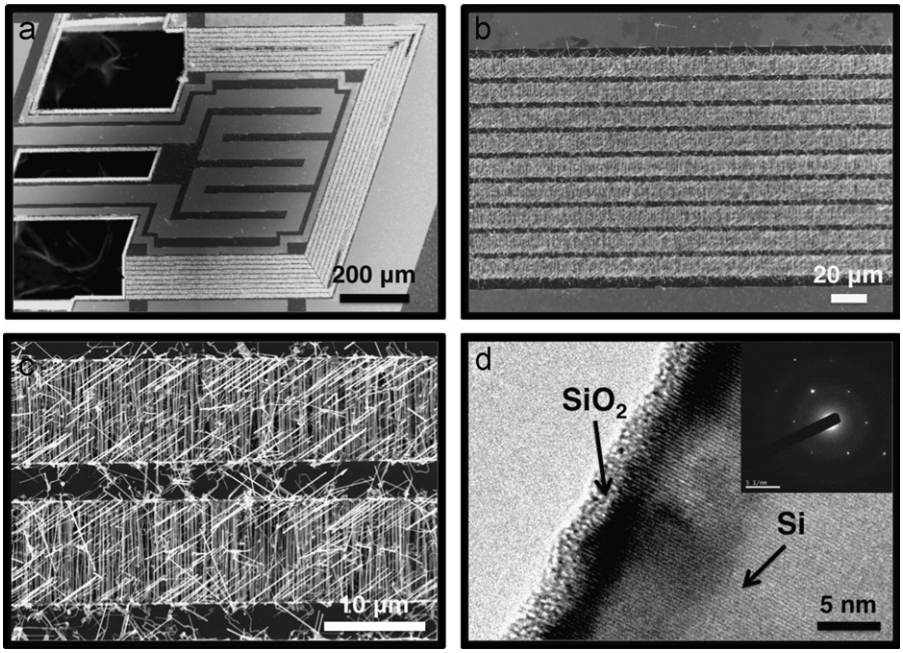

Figure 3 Multiple ordered arrays of silicon nanowires linked by silicon microspacers. (a) SEM image of a device with an integrated heater and silicon microspacers linking nine 10 μm-long nanowire arrays; (b) top view of nine silicon nanowire arrays connected through silicon microspacers, a detail is shown in (c); (d) high-resolution TEM image of a single crystal Si NW showing an amorphous external SiO_2 native layer.

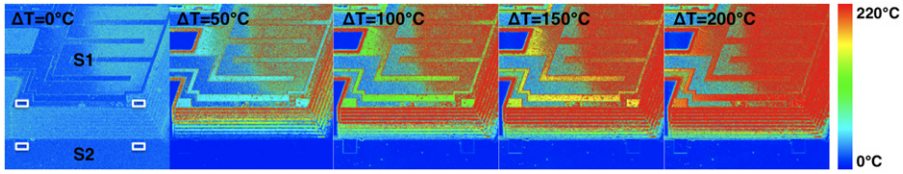

Figure 4 Thermoreflectance images of a device with 9 arrays of Si NWs transversally linked. Two-dimensional thermal images were acquired to observe the distribution of temperature changes corresponding to different temperatures attained above room temperature in the suspended platform using the heater. The areas highlighted by the white squares in the ΔT=0 °C image show the regions where the mean temperatures were measured. The image shows the silicon nanowire array acting as thermal barrier.

prior to the characterization of the devices. The thermal gradients to which the devices were subjected for its characterization were generated by two different methods: i) by means of an external hot-plate simulating a waste heat source (harvesting mode operation); ii) by means of the integrated heater.

In order to estimate the temperature differences attained during the characterization of the devices when employing the patterned heaters, it was necessary to determine the temperatures both in the suspended platform (S1) and the surrounding silicon bulk (S2). The surface temperature distribution was acquired by means of the thermoreflectance imaging technique, which utilizes the temperature dependence of the surface reflectivity of materials to determine the surface temperature changes when subjected to a modulated thermal excitation [29,30]. Figure 4 shows the distribution of temperature observed in the hot (S1) and cold (S2) regions of a device containing 9 Si NW arrays transversally linked, corresponding to different mean temperatures imposed through the heater. Clearly, the nanowires act as thermal barriers keeping the cold regions of the device (S2) nearly at room temperature with an increment of only 5 °C for the highest platform mean temperature imposed in the device (ΔT=200 °C). Therefore, the temperature difference ($T_{S2}-T_{S1}$) attained across the silicon nanowires can be approximated by the platform mean temperature measured through the heater TCR (see Appendix A in the supplementary info for a detailed explanation of the temperature gradient determination).

For a fixed temperature of the waste heat source (harvesting mode operation), an increase of more than 60% in the thermal gradient generated was achieved when comparing 1 array and 9 arrays of silicon nanowires (see Appendix A). Therefore, the longer the effective length of the metamaterial, the more thermally isolated the suspended platforms (S1) and therefore the higher the thermal gradient naturally generated. This confirms that using multiple linked arrays of nanowires is a good approach for a significant performance enhancement in harvesting applications.

Although the silicon-based metamaterial increases its thermal resistance by consecutively bridging more Si NW

arrays, its electrical resistance is not significantly affected. It is worth noting here that the density of the Si NW arrays was estimated to be 40 nanowires per square micron, meaning that a single device can contain several millions of nanowires. This parallel association of electrical resistances in combination with the quasi-epitaxial growth provided by the CVD-VLS growth technique, that virtually reduces to zero the contact resistance associated to the Silicon walls–Silicon NWs interface, makes the metamaterial electrical resistance almost negligible in all the cases. In fact, low internal resistances in the range of 35–70 Ω were measured for all the fabricated thermoelements without a defined trend with the number of microspacers, suggesting that these resistances are not directly attributable to the silicon nanowires. In addition, silicon-metal contact resistances were evaluated by using test structures yielding very low values on the order of 5–6 Ω. Metal strips used as current collectors are the main contributions to the total value of resistance. Therefore, improved design of the metal pads of the system will significantly reduce the internal resistance in the next generation of μTEGs.

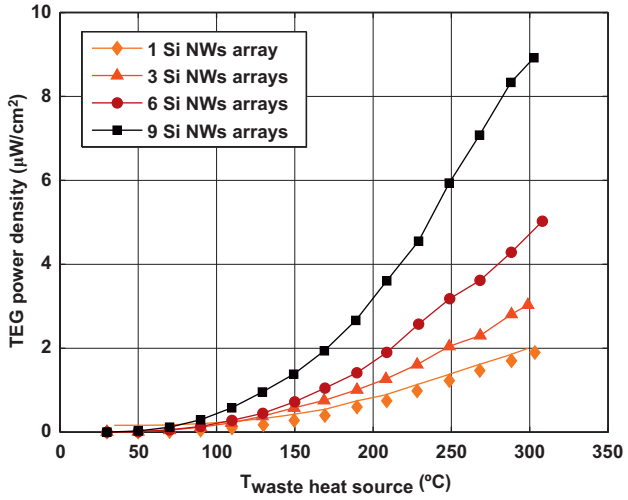

Figure 5 Thermoelectric power output in harvesting mode operation. Results obtained with structures containing different amounts of Si NW arrays (1, 3, 6 and 9). The graph shows the evolution of the maximum power densities generated by each thermoelement (TEG power), obtained from the I-V characteristic curves measured for waste heat source temperatures up to 300 °C.

From an energy generation perspective, power curves were measured in devices containing 1, 3, 6 and 9 Si NW arrays when placed on an external hot-plate kept at 300 °C. The maximum power generated in all cases is shown in Figure 5, confirming our performance enhancement strategy. As a best-case result, a maximum Seebeck voltage of 4.4 mV and a power density of 9 μW/cm^2 were measured for 9 arrays of Si NWs when placed on a heat source at 300 °C (ΔT=27 °C, across the metamaterial). These thermal gradient and power output values are greater by a factor of 30 and 3, respectively, when compared with a more complex top-down vertical structure based on silicon nanowires and consisting of 162 thermocouples recently reported by Li et al. [31].

In order to test the full extent of the potentiality of the μTEG as energy harvesters, the heater patterned in the suspended platform (S1) was employed to evaluate the performance when the structures were subjected to higher temperature differences. As previously mentioned, this scheme allows a full control of the temperature difference across the device and across the nanowires themselves. Figure 6 shows the evolution of the I-V and power curves measured at different temperature gradients for a structure

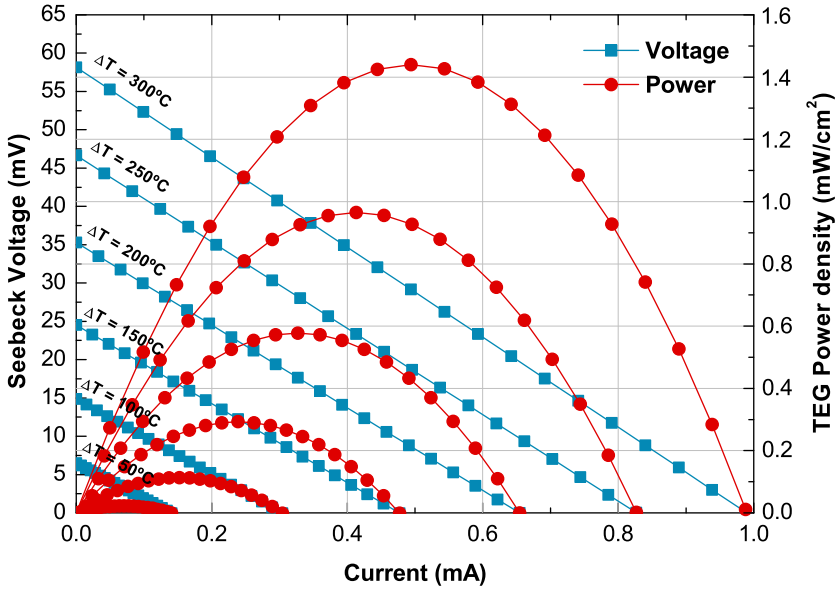

Figure 6 I-V and power density measurements at high temperature differences. I-V and power curves measured as a function of the temperature difference attained in a structure containing 9 Si NW arrays consecutively bridged. The power generated by the thermoelement (TEG Power) was obtained by measuring the generated voltages as a function of current for diverse temperature differences (ΔT), which were achieved by applying a DC current to the heater integrated in the structures.

Table 1 Comparison of the results obtained in this work with the state-of-the-art of thermoelectric microgenerators (adapted from [6]).

Company	Thermoelectric material	ΔT (K)	No. of couples	Power density (mW/cm^2)	P dens./couple ($\mu W/cm^2$)
DTS	$(Bi_{0.25}Sb_{0.75})Te_3/Bi_2(Te_{0.9}Se_{0.1})_3$	5	2250	0.0025	0.0011
JPL/NASA	$(Bi_{1-x}Sb_x)_2Te_3/Bi_2Te_3$	1.25	63	0.0346	0.5492
Micropelt	Bi_2Te_3	5	12	0.06	5
Micropelt	Bi_2Te_3	5	540	3.57[a]	6.611
Nextreme	Bi_2Te_3/Sb_2Te_3	10	N/A	14.66[b]	N/A
Infineon	Poly-Silicon	10	16000	0.0016	0.0001
HSG-IMIT and Kundo	Si/Al	10	1000	0.035	0.035
NUS	Top-down Si NWs	0.12	162	0.000006[c]	0.000037
This work	Bottom-up Si NW arrays	50	1	0.023	23
This work	Bottom-up Si NW arrays	300	1	1.44	1440

[a]Simulated power output [32].
[b]Taken from a preliminary data sheet [33].
[c]Not a commercially available product [31].

containing a metamaterial consisting of 9 Si NW arrays consecutively bridged. In this case, a maximum Seebeck voltage value of 58 mV and a maximum power density of 1.44 mW/cm^2 were measured at a temperature difference of 300 °C. These high values demonstrate that situations in which higher internal thermal gradients could be accomplished (*e.g.* by improved designs, forced convention refrigeration and/or engineering a heat spreader attached to the cold part) make this device an excellent harvester.

Table 1 shows a comparison between the thermoelements developed throughout this work and the state-of-the-art of thermoelectric microgenerators. Power densities were calculated by dividing the output power values by the area of the device in each case (1 mm^2 for the thermoelement developed in this work). Since the microgenerator developed here is based on a single thermoelement, opposite to the other references where the devices consist of several units, the table includes the power density by thermocouple. According to this table, the generated output power of devices based on V-VI semiconductor compounds is in general clearly higher than those generated by Si-based μTEGs (including the one developed for this work). However, the thermoelement fabricated here is well positioned when compared to other Si-based devices and when comparing the power density per couple obtained.

Additionally, different optimizations can be anticipated for future generations of our novel μTEG. Concerning materials aspects, tailoring the nanowire growth to increase the nanowires density, reduce the diameter and make the surfaces rougher could lead to the improvement of the thermoelectrical properties of the metamaterial. Concerning design issues, internal resistance reduction with improved metal pads and specific harvesting oriented configurations will improve the power output and thermal gradient, respectively. This future optimization, added to the intrinsic possibility of overcoming the thermal constrains that limit classical vertical configurations (limited ΔT) in the planar device architecture employed here, opens excellent perspectives for the successive generations of this novel device.

Finally, compared to μTEGs based on V-VI semiconductors, the device developed in this work is compatible with standard microtechnology processes and employs nanostructured silicon as the thermoelectric material. This gives a high design flexibility that allows moving from a radical miniaturization for nanodevices to a 3-D assembly able to generate up to 1 mW/cm^3 at low ΔT (<50 °C) and 50 mW/cm^3 at high ΔT (<300 °C) that will make this technology competitive with classical piezoelectric or electromagnetic generators.

Conclusions

The enhanced performance of thermoelectric generators by means of transversally linked Si NW arrays has been demonstrated for harvesting applications. This novel design exploits the simplicity of the 3D lateral growth of VLS-CVD Si NWs through an approach that enables obtaining effective arbitrary long Si NW-based metamaterials combined with a device architecture that preserves its electrical connectivity. Consecutively bridging multiple ordered Si NW arrays in a planar architecture has been shown to be a design solution that overcomes the technological limitation of the maximum thermoelement height, i.e. maximum temperature gradient attainable, arising when traditional vertical configurations are reproduced in the microscale. It should be also stressed that the results presented here correspond to the behavior of a single thermocouple structure. Due to its full technological compatibility with standard microelectronic fabrication processes, a large number of these thermocouples could be packaged and appropriately connected in a single chip for the generation of higher power devices (controlling voltage or current). This high integrability, together with future modification of Si NWs morphology already known to improve their intrinsic thermoelectrical properties (smaller diameter, rougher surface, etc.) opens excellent perspectives for successive generations of this device. Furthermore, current thermoelectric generators based on V-VI semiconductors, although showing better performances, suffer from a short-

term near-critical supply risk of raw materials like Tellurium that will make them less competitive in the next two decades [8]. Therefore, we anticipate that the results presented in this work could bring a new silicon-based thermoelectric generation technology closer to practical implementation of μTEGs in local energy supply applications such as wireless sensor networks and remote actuators or advanced micro/nanodevices.

Acknowledgments

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Appendix A. Supporting information

Supplementary data associated with this article can be found in the online version at http://dx.doi.org/10.1016/j.nanoen.2012.06.006.

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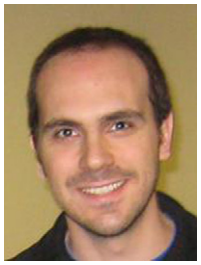
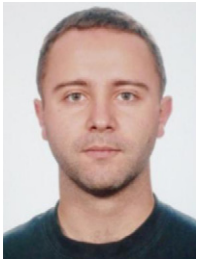


Albert Tarancón is a Senior Scientist and Head of the Nanoionics and Fuel Cells Group of the Advanced Materials for Energy Department at the Catalonia Institute for Energy Research (IREC). His research interest is primarily concerned with materials for alternative energy technologies and their applicability in powering portable devices. Particular fields of interest are the integration of nanoionics concepts in micro Solid Oxide Fuel Cells and silicon nanowires in thermoelectric microgenerators.

Carlos Calaza received his B.S. degree in Physics from the University of Santiago de Compostela in 1996 and his BS degree in Electronic Engineering and his Ph.D. in Physics from the University of Barcelona in 2000 and 2003, respectively. In 2003 he joined the ITC-irst in Trento, Italy as a postdoctoral researcher, working on the development of MEMS devices for several applications. Since 2009 he is working at the Microelectronics Institute of Barcelona (IMB-CNM, CSIC), where his actual research interest is focused on technological innovations for silicon based optical chemical sensing and thermoelectric energy microgeneration.



Marc Salleras received a B.S. in physics and electronics engineering from the Universitat de Barcelona in 1999 and 2002 respectively, and the Ph.D. degree in physics from the same university in 2007. After that he spent more than two years as a postdoctoral scholar at the University of California at Irvine working on MEMS gyroscopes. Since 2009 he is a postdoctoral researcher at National Microelectronics Center in Barcelona. His research is focused on the design, modelling and simulation of MEMS devices.

Marta Fernández-Regúlez received her B.Sc. and M.S. degrees in Physics from the Universidad de Valladolid, Spain. Currently, she is pursuing her Ph.D. in Electronic Engineering under the supervision of Dr. Alvaro San Paulo at the Instituto de Microelectronica de Barcelona IMB-CNM (CSIC). Her current research is focused towards the development of high yield fabrication technologies based on catalyst grown Si nanowires to develop devices that exploit their exceptional properties.

Alvaro San Paulo received the Ph.D. Degree in Physics from the Universidad Autonoma de Madrid in 2002. Then he joined the EECS Division of the University of California at Berkeley as a postdoctoral researcher until 2006. In 2006 he moved to the Instituto de Microelectronica de Barcelona (CSIC) with a Ramon y Cajal Research Contract. In December 2007 he earned a permanent research position at CSIC. In 2011 he moved to the Instituto de Microelectronica de Madrid (CSIC). His scientific contributions to date are related to nanomechanics and nanofabrication, and his most important achievements have been made in the specific areas of atomic force microscopy and Si nanowire growth-based nanofabrication.

Luis Fonseca was born in Barcelona, Spain, in 1966. He received his B.S. and Ph.D. degrees in Physics from the Autonomous University of Barcelona in 1988 and 1992, respectively. In 1989 he joined the National Center of Microelectronics as a post-graduate student, working till 1992 on the growth and characterization of thin dielectric films for VLSI and ULSI applications. After this first research period he worked as a process engineer, leading the diffusion and deposition areas of the CNM production facilities. In 2001 he joined the Microsystems group as a full senior researcher being his research area focused on technological developments for gas sensing and more specifically on optical gas sensing. He is presently involved as well in the development of micro and nanotechnologies for thermoelectricity.